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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,061	BANERJEE ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-46 are pending.

Papers Filed

2. Examiner acknowledges receipt RCE with remarks and amendments filed on 19 October 2006.

Title

3. The title is accepted. Objection is withdrawn.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 23-30 and 45-46 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. An amendment filed by Applicant on May 30th, 2006 has limited these claims to "computer readable storage medium"; however, Applicant's current specification does not particular distinguish a storage medium from a transmission medium. Examiner recommends the following change to paragraph [0068] of Applicant's specification to clarify the issue:

> *Such software can be disposed in any known computer usable storage medium including semiconductor, magnetic disk, optical disc (e.g., CD-ROM, DVD-ROM, etc.) ~~and~~ or as a computer data signal embodied in a computer usable (e.g., readable) transmission medium (e.g., carrier wave or any other medium including*

digital, optical, or analog-based medium). As such, the software can be transmitted over communication networks including the Internet and intranets.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (U.S. Patent No. 6,167,505) in view of Computer Organization and Design (herein Hennessy)

3. As per claim 1, Kubota discloses an instruction fetch unit for a processor, comprising:

a first recoder; (Fig. 2 decoder 160)

and a second recoder (Fig. 2 Ext registers 172 and 174 in combination with Immediate Generation Circuit 170) coupled to the first recoder, *The examiner asserts that the recoders are coupled by means of the bus shown in Fig. 2.*

wherein the first recoder passes information regarding a first instruction (prefix instruction) to the second recoder, and the second recoder recodes a second instruction (target instruction) based on the information passed by the first recoder. (Col. 9 lines 19-36 and lines 52-57)

Kubota fails to disclose conclusively a second instruction sent through a second recorder so as to map the second instruction from a first encoded state to a second

encoded state. This limitation appears to require that a decoder to be present after the recoder.

Examiner asserts that Kubota fig. 2 references 160, , 170, 172, 174 appear to disclose all the requirements of a "recoder" as claimed. Upon further analysis of fig. 2, these recoded instructions are outputted through a series of wires/logic and later enter the ALU 190. Examiner asserts that, more than likely, an actual implementation of fig. 2 requires more logic than is shown. However, because details are sparse, a further reference will be used.

Hennessy discloses that, "the process of branching to different states depending on the instruction is called decoding" (page 392). To further illustrate the decoding process of Hennessy, Fig. 5.42 on page 396 shows in the upper right, some of the determinations made in the instruction decode stage. In particular, based on the Operation code ("Op") the type of instruction is determined and, from there, various control signals for the ALU are determined. These signals control the operation of the ALU and are required for proper implementation.

Applicant's attention is directed to fig. 5.48 of page 414. This is a processing unit for a typical 5-stage pipeline that includes 1) Instruction Fetch, 2) Instruction Decode (with register reads), 3) Execution, 4) Memory Read/Write, 5) Write Back. Much of the decoding process occurs between the box labeled "Memory" and the "ALU". As described above, the instruction in Operation Code (here, Instruction [31-26] or Op [5-0]) is used to create the control signals in the box "Control". This is part of the decoding process.

Looking again at Kubota Fig. 2, the instructions are accessed from memory they are moved into a recoder, and then enter the ALU. Likely, Kubota intended to have these encoded outputs decoded into control signals at some point before they enter the ALU. In fact, this the only option known to Examiner. Either way, Kubota would be motivated to utilize the control signal generation decoding as shown in Hennessy in order to utilize an efficient, well-established method for executing instructions in an ALU.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing unit of Kubota and combine it with Hennessy in such a way that instructions, once recoded (and still in encoded from) travel the a decoding unit that creates control signals for ALU operation and, once decoded, is properly executed in ALU 190.

6. As per claim 2, Kubota/Hennessy discloses the instruction fetch unit of claim 1, further comprising: an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder. *The examiner asserts that there must inherently exist a dispatch unit to move instructions from instruction register 150 (Fig. 2) to the recoders (decoder 160 and combination of parts 170, 172, 174). Without a means to dispatch an instruction to either of the decoders, no instruction would be able to be executed in Kubota's system.*

7. As per claim 3, Kubota/Hennessy discloses the instruction fetch unit of claim 1, wherein the processor executes instructions having X-bits and belonging to a first instruction set (instructions having 16-bits of length. Examples pictured in Figs. 7 and 9) and instructions having Y-bits and belonging to a second instruction set (Instructions having 32-bits of length. Examples pictured in Figs. 8 and 10), Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits. (Col. 9 line 58 – col. 10 line 12)

8. As per claim 4, Kubota/Hennessy discloses the instruction fetch unit of claim 3, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits. (Col. 9 line 58 – col. 10 line 12)

9. As per claim 5, Kubota/Hennessy discloses the instruction fetch unit of claim 3, wherein the first instruction set includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set, (Col. 8 lines 43-49) and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction. (Col. 10 lines 20-26)

10. As per claim 6, Kubota/Hennessy discloses the instruction fetch unit of claim 5, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction. (Col. 10 lines 9-13)

11. As per claim 7, Kubota/Hennessy discloses the instruction fetch unit of claim 3, wherein the first instruction set includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction. (Col. 18 lines 48-67) *The examiner asserts that a branch instruction constitutes a mode-switch instruction as the flow of a program switches along with the processor taking the branch path.*

12. As per claim 8, Kubota/Hennessy discloses the instruction fetch unit of claim 7, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction. (Col. 18 lines 48-67)

13. As per claim 9, Kubota/Hennessy has taught a processor employing the fetch unit of claim 1, consequently claim 9 is rejected for the same reasons set forth in the rejection of claim 1 above.

14. As per claim 10, Kubota/Hennessy has taught a processor employing the fetch unit of claim 2, consequently claim 10 is rejected for the same reasons set forth in the rejection of claim 2 above.

15. As per claim 11, Kubota/Hennessy has taught a processor employing the fetch unit of claim 3, consequently claim 11 is rejected for the same reasons set forth in the rejection of claim 3 above.

16. As per claim 12, Kubota/Hennessy has taught a processor employing the fetch unit of claim 4, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 4 above.

17. As per claim 13, Kubota/Hennessy has taught a processor employing the fetch unit of claim 5, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 5 above.

18. As per claim 14, Kubota/Hennessy has taught a processor employing the fetch unit of claim 6, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 6 above.

19. As per claim 15, Kubota/Hennessy has taught a processor employing the fetch unit of claim 7, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 7 above.

20. As per claim 16, Kubota/Hennessy has taught a processor employing the fetch unit of claim 8, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 8 above.

21. As per claim 17, Kubota/Hennessy has taught a processing system employing the fetch unit of claim 1, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 1 above.

22. As per claim 18, Kubota/Hennessy has taught a processing system employing the fetch unit of claim 2, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 2 above.

23. As per claim 19, Kubota/Hennessy has taught a processing system employing the fetch unit of claim 3, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 3 above.

24. As per claim 20, Kubota/Hennessy has taught a processing system employing the fetch unit of claim 4, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 4 above.

25. As per claim 21, Kubota/Hennessy has taught a processing system employing the fetch unit of claim 5, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 5 above.

26. As per claim 22, Kubota/Hennessy has taught a processing system employing the fetch unit of claim 6, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 6 above.

27. As per claim 23, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 1, consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 1 above.

28. As per claim 24, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 2, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 2 above.

29. As per claim 25, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 3, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 3 above.

30. As per claim 26, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 4, consequently claim 26 is rejected for the same reasons set forth in the rejection of claim 4 above.

31. As per claim 27, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 5, consequently claim 27 is rejected for the same reasons set forth in the rejection of claim 5 above.

32. As per claim 28, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 6, consequently claim 28 is rejected for the same reasons set forth in the rejection of claim 6 above.

33. As per claim 29, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 7, consequently claim 29 is rejected for the same reasons set forth in the rejection of claim 7 above.

34. As per claim 30, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 8, consequently claim 30 is rejected for the same reasons set forth in the rejection of claim 8 above.

35. As per claim 31, Kubota/Hennessy discloses a method for recoding instructions for execution by a computer readable medium comprising a microprocessor core, comprising:

(a) fetching an expand instruction (prefix instruction) and an expandable instruction (target instruction) from an instruction cache; *The examiner asserts that there must inherently exist a dispatch unit to move instructions from instruction register 150 (Fig. 2) to the recoders (decoder 160 and combination of parts 170, 172, 174). Without a means to dispatch an instruction to either of the decoders, no instruction would be able to be executed in Kubota's system.*

(b) dispatching the expand instruction to a first recoder and dispatching the expandable instruction to a second recoder; (Col. 9 lines 19-36 and lines 52-57)

(c) generating at the first recoder at least one information bit based on the expand instruction; (Col. 10 lines 20-26) *The examiner asserts that the immediate data is generated from the first instruction in order for it to be passed to the second recoder.*

and (d) recoding the expandable instruction at the second recoder using the at least one information bit generated at the first recoder. (Col. 10 lines 20-26). *The examiner asserts that the second recoder recodes the second instruction by adding the data from the first instruction to an immediate field in the seond.*

36. As per claim 32, Kubota/Hennessy discloses the method of claim 31, wherein step (a) comprises:

(i) fetching the expand instruction during a first clock cycle of the computer readable medium comprising a microprocessor core; and

(ii) fetching the expandable instruction during a subsequent clock cycle of the computer readable medium comprising a microprocessor core. *Fig. 5 depicts fetching an EXT instruction (prefix instruction) in clock cycle number 2 and an LD instruction (target instruction) in the subsequent clock cycle.*

37. As per claim 33, Kubota/Hennessy discloses the method of claim 31, wherein the at least one information bit based on the expand instruction is generated at the first recoder during a first clock cycle of the processor, and the expandable instruction is recoded at the second recoder during a second clock cycle of the computer readable medium comprising a microprocessor core. *Fig. 5 depicts fetching an EXT instruction (prefix instruction) in clock cycle number 2 and an LD instruction (target instruction) in the subsequent clock cycle. When the EXT_LOW signal 550 is high in clock cycle number three, the data from the target instruction is combined with the data from the previous EXT instruction (col. 12 lines 21-31).*

38. As per claim 34, Kubota/Hennessy discloses the method of claim 33, further comprising a step between steps (c) and (d) of:

storing the at least one information bit generated at the first recoder in an information storage buffer. *The examiner asserts that registers EXT1 and EXT2 (Fig. 2) constitute storage buffers. Col. 12 lines 21-31 indicate that data has been stored therein.*

39. As per claim 35, Kubota/Hennessy discloses a method for recoding instructions for execution by a processor, comprising:

fetching a plurality of instructions from an instruction cache (Fig. 2 instruction register 150), wherein the plurality of instructions includes a first instruction (prefix instruction) and a second instruction (target instruction), and the first instruction is different from the second instruction; *The examiner asserts that the instructions must inherently be fetched before being decoded.*

dispatching the first instruction to a first recoder and the second instruction to a second recoder; (Col. 9 lines 19-36 and lines 52-57)

and recoding the first and second instructions within a single clock cycle. *The examiner asserts that there exists a single clock cycle in which the results of the combination of immediate data from the first and second instructions becomes valid. This is the cycle in which the instructions are considered to be "recoded."*

40. As per claim 36, Kubota/Hennessy discloses the method of claim 35, wherein the recoding of the second instruction is performed using information from the first instruction. (Col. 12 lines 21-31)

41. As per claim 37, Kubota/Hennessy discloses the method of claim 35, further comprising forwarding information from the first recoder to the second recoder, such information used by the second recoder to perform a recoding operation. (Col. 12 lines 21-31)

42. As per claim 38, Kubota/Hennessy discloses an instruction fetch unit for a processor comprising:

a first recoder (Fig. 2 decoder 160);

and a second recoder (Fig. 2 Ext registers 172 and 174 in combination with Immediate Generation Circuit 170) which operates in parallel with the first recoder;

wherein the first recoder recodes a first instruction and the second recoder recodes a second instruction within a single clock cycle, and the first instruction is different from the second instruction. (Col. 9 lines 19-36 and lines 52-57) *The examiner asserts that there exists a single clock cycle in which the results of the combination of immediate data from the first and second instructions becomes valid. This is the cycle in which the instructions are considered to be "recoded."*

43. As per claim 39, Kubota/Hennessy discloses the instruction fetch unit of claim 38, wherein the second recoder recodes the second instruction using information from the first instruction. (Col. 12 lines 21-31)

44. As per claim 40, Kubota/Hennessy discloses the instruction fetch unit of claim 39, wherein the first recoder is coupled to the second recoder. *Fig. 2 discloses the two recoders being coupled together by means of a bus.*

45. As per claim 41, Kubota/Hennessy discloses the instruction fetch unit of claim 1, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction. (Col. 9 lines 19-36 and lines 52-57)

46. As per claim 42, Kubota/Hennessy discloses the instruction fetch unit of claim 41, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field. (Col. 9 lines 19-36 and lines 52-57)

47. As per claim 43, Kubota/Hennessy has taught a processor employing the fetch unit of claim 41, consequently claim 43 is rejected for the same reasons set forth in the rejection of claim 41 above.

48. As per claim 44, Kubota/Hennessy has taught a processor employing the fetch unit of claim 42, consequently claim 44 is rejected for the same reasons set forth in the rejection of claim 42 above.

49. As per claim 45, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 41, consequently claim 45 is rejected for the same reasons set forth in the rejection of claim 41 above.

4. As per claim 46, Kubota/Hennessy has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 42, consequently claim 46 is rejected for the same reasons set forth in the rejection of claim 42 above.

Response to Arguments

5. Applicant's arguments filed 19 October 2006 have been fully considered but they are not persuasive.

6. Applicant states:

"Claims 23-30, 45 and 56 are directed to a tangible computer readable storage medium comprising a microprocessor core embodied in software. In 1995, the Commissioner of Patents and Trademarks conceded to the U.S. Court of Appeals for the Federal Circuit "that computer programs embodied in a tangible medium, such as a floppy diskettes, are patentable subject matter under 35 U.S.C. 101."

Examiner finds this argument unpersuasive. The claim language in light of the specification still encompasses computer usable transmission medium. The solution, as suggested above, is to amend the specification to label the examples listed in two distinct categories: computer usable storage medium and computer usable transmission

medium. Since the rejected claims clearly only refer to a "computer readable storage medium" then this amendment will prevent the claims from encompassing the examples written under the computer usable transmission medium, such as a carrier wave.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
PRIMARY EXAMINER